

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88506	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	68901-4	Multifunction peripheral (4 mHz)
02	68901-5	Multifunction peripheral (5 mHz)

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-14 (48-lead, 2.435" x .620" x .225"), dual-in-line package
Y	C-6 (52-terminal, .750" x .750"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.3 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.5 W
Lead temperature (soldering, 5 seconds)	+270°C
Junction temperature (T_J)	+170°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X and Y	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage:	
V_{CC}	4.75 V dc to 5.25 V dc
V_{SS}	0 V
High level input voltage (logic inputs) (V_{IH})	2.0 V to V_{CC}
Low level input voltage (logic inputs) (V_{IL})	GND to 0.8 V dc
Minimum high level output voltage	2.4 V dc
Maximum low level output voltage	0.5 V dc
Frequency of operation:	
Device type 01	1.0 to 4.0 MHz
Device type 02	1.0 to 5.0 MHz
Case operating temperature range (T_C)	-55°C to +125°C

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C < +125°C 1/ V _{CC} = 5 V ±5% unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Power supply current outputs open	I _{CC}	V _{CC} = 5.25 V	1,2,3		180	mA
Low level output voltage (except DTACK)	V _{OL}	I _{OL} = 2.0 mA, V _{CC} = 4.75 V	1,2,3		0.5	V
High level output voltage (except DTACK)	V _{OH}	I _{OH} = -120 μA, V _{CC} = 4.75 V	1,2,3	2.4		V
DTACK output source current	I _{OH}	V _{OUT} = 2.4 V	1,2,3		-400	μA
DTACK output sink current	I _{OL}	V _{OUT} = 0.5 V	1,2,3		5.3	mA
Input leakage current	I _{IM}	V _{IN} = 0 to 5.25 V	1,2,3	-10	+10	μA
Three-state output current in float	I _{LOH}	V _{OUT} = 2.4 to V _{CC}	1,2,3		+10	μA
Three-state output current in float	I _{LOL}	V _{OUT} = 0.5 V	1,2,3		-10	μA
High level input voltage (all inputs)	V _{IH}		1,2,3	2.0	V _{CC} +0.3	V
Low level input voltage (all inputs)	V _{IL}		1,2,3	-0.3	0.8	V
Input capacitance	C _{IN}	See 4.3.1c	4		10	pF
Three-state output capacitance	C _{OUT}	See 4.3.1c	4		10	pF
Functional tests		See 4.3.1d	7,8			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5 V ±5% unless otherwise specified	Reference number	Group A subgroups	Limits				Unit
					Min	Max	Min	Max	
					4.0 MHz		5.0 MHz		
CS, DS width high	t _{SWH}	2/	1	9,10,11	50		35		ns
R/W, A ₁ -A ₅ valid to falling CS (setup)	t _{RASL}		2	9,10,11	0		0		ns
Data valid prior to falling CLK	t _{DVCL}		3	9,10,11	0		0		ns
CS, IACK valid prior to falling CLK (setup)	t _{SVCL}	3/	4	9,10,11	50		45		ns
CLK low to DTACK low	t _{CLDL}		5	9,10,11		220		180	ns
CS, DS or IACK high to DTACK high	t _{SHDH}	4/	6	9,10,11		60		55	ns
CS, DS or IACK high to DTACK three-state	t _{SHDZ}		7	9,10,11		100		95	ns
DTACK low to data invalid (hold time)	t _{DLDI}		8	9,10,11	0		0		ns
CS, DS or IACK high to data three state	t _{SHDZ}	4/	9	9,10,11		100		100	ns
CS or DS high to R/W A ₁ -A ₅ invalid (hold time)	t _{SHRAZ}		10	9,10,11	0		0		ns
Data valid from CS low	t _{DVSL}	3/ 5/	11	9,10,11		310		260	ns
Read data valid to DTACK low (setup time)	t _{RDVCL}		12	9,10,11	50		50		ns
DTACK low to DS, CS or IACK high (hold time)	t _{DLSH}		13	9,10,11	0		0		ns
IET low to falling CLK (setup time)	t _{ILCL}		14	9,10,11	50		50		ns
IEO valid from CLK low (delay)	t _{IVCL}	4/	15	9,10,11		180		180	ns
Data valid from CLK low (delay)	t _{DAVCL}		16	9,10,11		300		300	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5 V ±5% unless otherwise specified	Refer- ence number	Group A subgroups	Limits				Unit
					Min	Max	Min	Max	
					4.0 MHz		5.0 MHz		
\overline{CEO} invalid from \overline{IACK} high (delay)	t _{IIH}		17	9,10,11		150		150	ns
\overline{DTACK} low from CLK high (delay)	t _{DLCH}		18	9,10,11		180		165	ns
\overline{CEO} valid from \overline{IET} low (delay)	t _{IVIL}	4/	19	9,10,11		100		100	ns
Data valid from \overline{IET} low (delay)	t _{DAVIL}		20	9,10,11		220		220	ns
CLK cycle time	t _{CT}		21	9,10,11	250	1000	200	1000	ns
CLK width low	t _{CL}	4/	22	9,10,11	110		90		ns
CLK width high	t _{CH}	6/	23	9,10,11	110		90		ns
\overline{CS} , \overline{IACK} inactive to rising CLK (setup)	t _{SICL}	2/ 7/	24	9,10,11	100		80		ns
I/O minimum active pulse width	t _{IOAW}		25	9,10,11	100		100		ns
\overline{IACK} width high	t _{IWH}	6/	26	9,10,11	2		2		t _{CLK}
I/O data valid from rising \overline{CS} or \overline{DS}	t _{IDVSL}		27	9,10,11		450		450	ns
Receiver ready delay from rising RC	t _{RRCL}		28	9,10,11		600		600	ns
Transmitter ready delay from rising TC	t _{TRCL}		29	9,10,11		600		600	ns
Timer output low from rising edge of \overline{CS} , \overline{DS}	t _{TLSH}	8/	30	9,10,11		450		450	ns
t _{OUT} valid from internal timeout	t _{VIT}	6/	31	9,10,11		2 t _{CLK} +300		2 t _{CLK} +300	ns
Timer CLK low time	t _{TCL}		32	9,10,11	110		90		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5 V ±5% unless otherwise specified	Refer- ence number	Group A subgroups	Limits				Unit
					Min	Max	Min	Max	
					4.0 MHz		5.0 MHz		
Timer CLK high time	t _{TCH}		33	9,10,11	110		90		ns
Timer CLK cycle time	t _{TCC}		34	9,10,11	250	1000	200	1000	ns
RESET low time	t _{RL}		35	9,10,11	2		1.8		μs
Delay to falling $\overline{\text{IRQ}}$ from external interrupt active transition	t _{DILI}		36	9,10,11		380		380	ns
Transmitter internal interrupt delay from falling TC	t _{TTCL}		37	9,10,11		550		550	ns
Receiver buffer full interrupt transition delay from rising RC	t _{RICL}		38	9,10,11		800		800	ns
Receiver error interrupt transition delay from falling edge of RC	t _{RIECL}		39	9,10,11		800		800	ns
Serial in setup time to to rising edge of RC (divide by one only)	t _{SRCL}		40	9,10,11	80		70		ns
Data hold time from rising edge of RC (divide by one only)	t _{DHRL}		41	9,10,11	350		325		ns
Serial output data valid from falling edge of TC (±1)	t _{DTCL}		42	9,10,11		440		420	ns
Transmitter CLK low time	t _{TACL}		43	9,10,11	500		450		ns
Transmitter CLK high time	t _{TACH}		44	9,10,11	500		450		ns
Transmitter CLK cycle time	t _{TACC}		45	9,10,11	1.05		0.95		μs
Receiver CLK lowtime	t _{RCL}		46	9,10,11	500		450		ns

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C < +125^{\circ}\text{C}$ $V_{CC} = 5\text{ V} \pm 5\%$ unless otherwise specified	Refer- ence number	Group A subgroups	Limits				Unit
					Min	Max	Min	Max	
					4.0 MHz		5.0 MHz		
Receiver CLK high time	t_{RCH}		47	9,10,11	500		450		ns
Receiver CLK cycle time	t_{RCC}		48	9,10,11	1.05		0.95		μs
$\overline{\text{CS}}$, $\overline{\text{IACK}}$, $\overline{\text{DS}}$ width low	t_{SWL}	6/	49	9,10,11		80		80	t_{CLK}
Serial output data valid from falling edge T_C (± 16)	t_{DATCL}		50	9,10,11		490		370	ns

1/ See figures 3 and 4.

2/ $\overline{\text{CS}}$ is latched internally, therefore if reference numbers 1 and 24 are met, then $\overline{\text{CS}}$ may be reasserted before the rising clock and still terminate the current bus cycle. The new bus cycle will be delayed by the device until all appropriate internal operations have completed.

3/ If the setup time is not met, $\overline{\text{CS}}$ or $\overline{\text{IACK}}$ will not be recognized until the next falling CLK.

4/ $\overline{\text{IEO}}$ only goes low if no acknowledgeable interrupt is pending. If $\overline{\text{IEO}}$ goes low, $\overline{\text{DTACK}}$ and the data bus remain three-stated.

5/ Although $\overline{\text{CS}}$ and $\overline{\text{DTACK}}$ are synchronized with the clock, the data out during a read cycle is asynchronous to the clock, relying only on $\overline{\text{CS}}$ for timing.

6/ t_{CLK} refers to the clock applied to the MFP CLK input pin. t_{CLK} refers to the timer clock signal, regardless of whether that signal comes from the XTAL1/XTAL2 crystal clock inputs or the TAI or TBI timer inputs.

7/ If this setup time is met (for consecutive cycles), the minimum hold-off time of one clock cycle will be obtained. If not met, the hold-off will be two clock cycles.

8/ Reference number 30 applies to timer outputs TAO and TBO only.

Timer ac characteristics

Definitions:

Error = Indicated time value - actual time value

$t_{psc} = t_{CLK} \times \text{prescale value}$

Internal timer mode:

Single interval error (free running) (see note 1) - $\pm 100\text{ ns}$

Cumulative internal error - - - - - 0

Error between two timer reads - - - - - $\pm (t_{psc} - 4 t_{CLK})$

Start timer to stop timer error - - - - - $2 t_{CLK} + 100\text{ ns}$ to $-(t_{psc} + 6 t_{CLK} + 100\text{ ns})$

Start timer to read timer error - - - - - 0 to $-(t_{psc} + 6 t_{CLK} + 400\text{ ns})$

Start timer to interrupt request error (see note 2) - $-2 t_{CLK}$ to $-(4 t_{CLK} + 800\text{ ns})$

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Pulse width measurement mode:

Measurement accuracy (see note 3) - - - - - 2 tCLK to -(t_{psc} + 4 tCLK)
Minimum pulse width - - - - - 4 tCLK

Event counter mode:

Minimum active time of TAI and TBI - - - - - 4 tCLK
Minimum inactive time of TAI and TBI - - - - - 4 tCLK

NOTES:

1. Error with respect to t_{OUT} or t_{RQ} if note 2 is true.
2. Assuming it is possible for the timer to make an interrupt request immediately.
3. Error may be cumulative if repetitively performed.

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Subgroups 7 and 8 shall verify the instruction set. The instruction set forms a part of the vendors' test tape and shall be maintained and available from the approved sources of supply.

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Case outline X

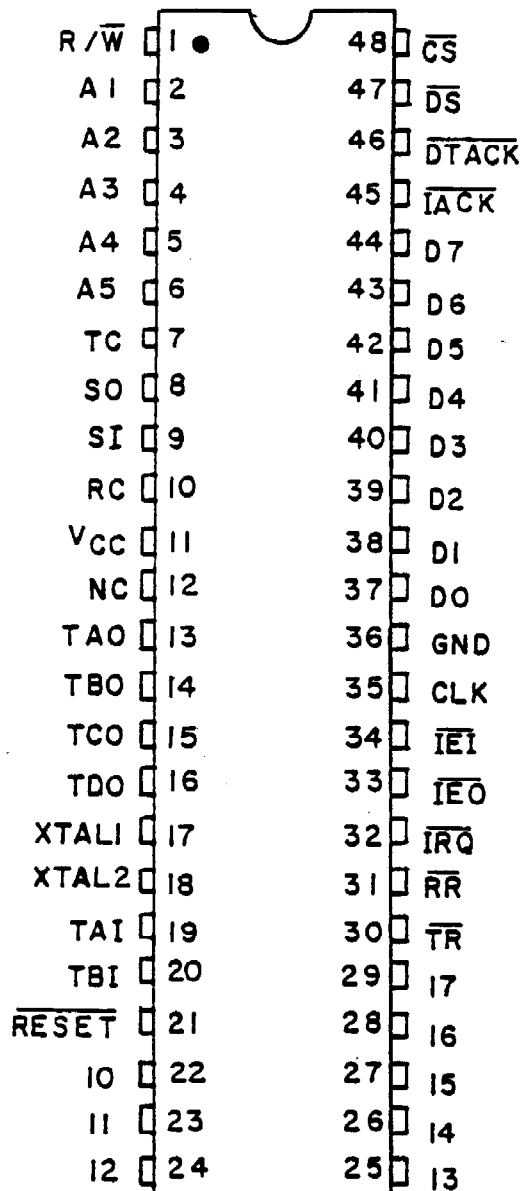


FIGURE 1. Terminal connections.

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Case outline Y

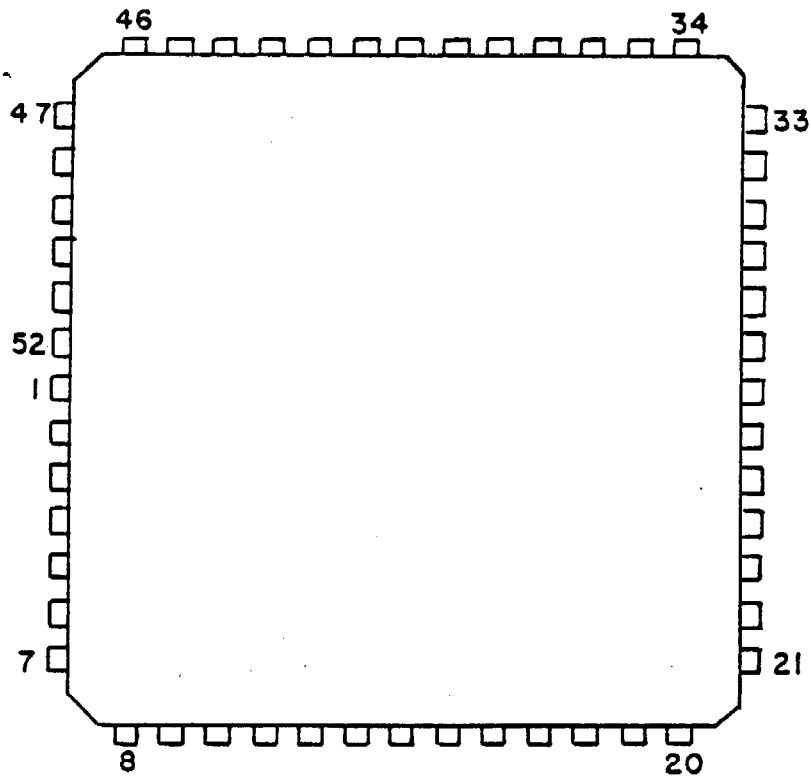


FIGURE 1. Terminal connections - Continued.

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Case outline Y

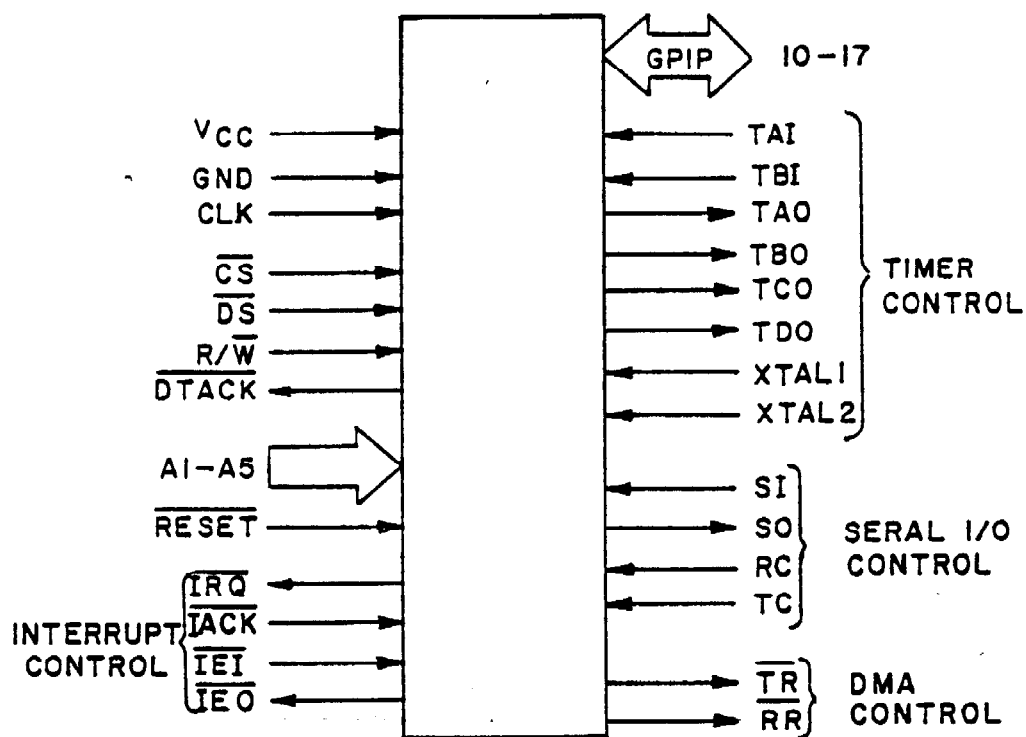
Pin connections

LCC	Func.	LCC	Func.	LCC	Func.
1	NC	19	XTAL1	37	TEO
2	R/W	20	XTAL2	38	TEI
3	A1	21	NC	39	CLK
4	A2	22	TAI	40	GND
5	A3	23	TBI	41	D0
6	A4	24	RESET	42	D1
7	A5	25	10	43	D2
8	TC	26	11	44	D3
9	S0	27	12	45	D4
10	SI	28	13	46	D5
11	RC	29	14	47	D6
12	VCC	30	15	48	D7
13	NC	31	16	49	TACK
14	NC	32	17	50	DTACK
15	TA0	33	NC	51	DS
16	TB0	34	TR	52	CS
17	TC0	35	RR		
18	TD0	36	TRQ		

NOTE: NC - no connection

FIGURE 1. Terminal connections - Continued.

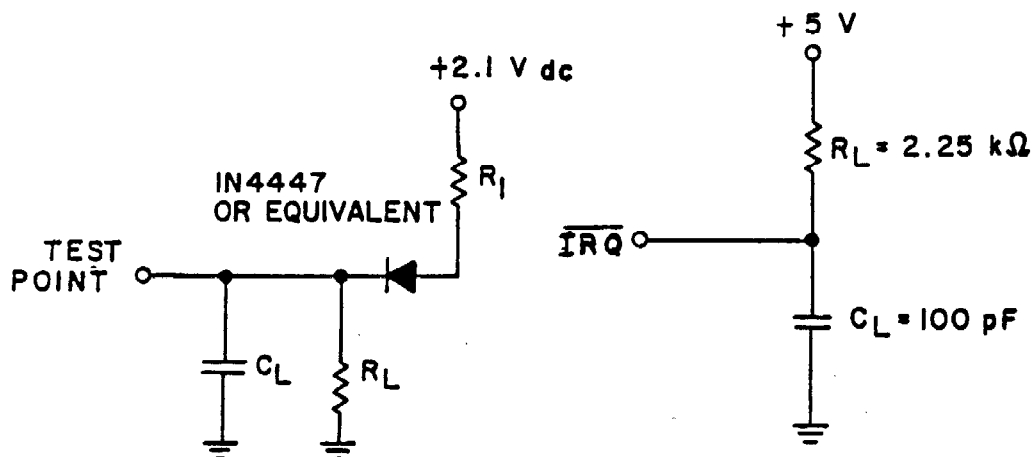
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Input and output signals

FIGURE 2. Block diagram.

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for all outputs except \overline{DTACK}

$$C_L = 100 \text{ pF}$$

$$R_L = 20 \text{ k}\Omega$$

$$R_1 = 180\Omega$$

for \overline{DTACK}

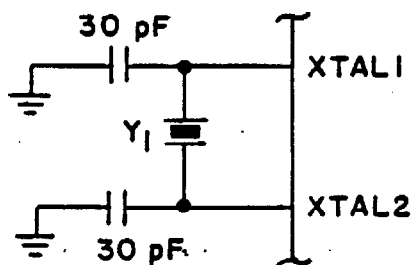
$$C_L = 130 \text{ pF}$$

$$R_L = 6 \text{ k}\Omega$$

$$R_1 = 470\Omega$$

Typical output

\overline{IRQ} test load



Y_1 (Crystal parameters):

Parallel resonance, fundamental mode AT cut

$R_S < 150\Omega$ (FR = 2.8 - 5.0 MHz):

$R_S < 300\Omega$ (FR = 2.0 - 2.7 MHz)

$C_L = 18 \text{ pF}$; $C_M = 0.02 \text{ pF}$; $C_h = 5 \text{ pF}$; $L_M = 96 \text{ mH}$

F_R (typ) = 2.4576 MHz

MFP external oscillator components

FIGURE 3. Test circuits.

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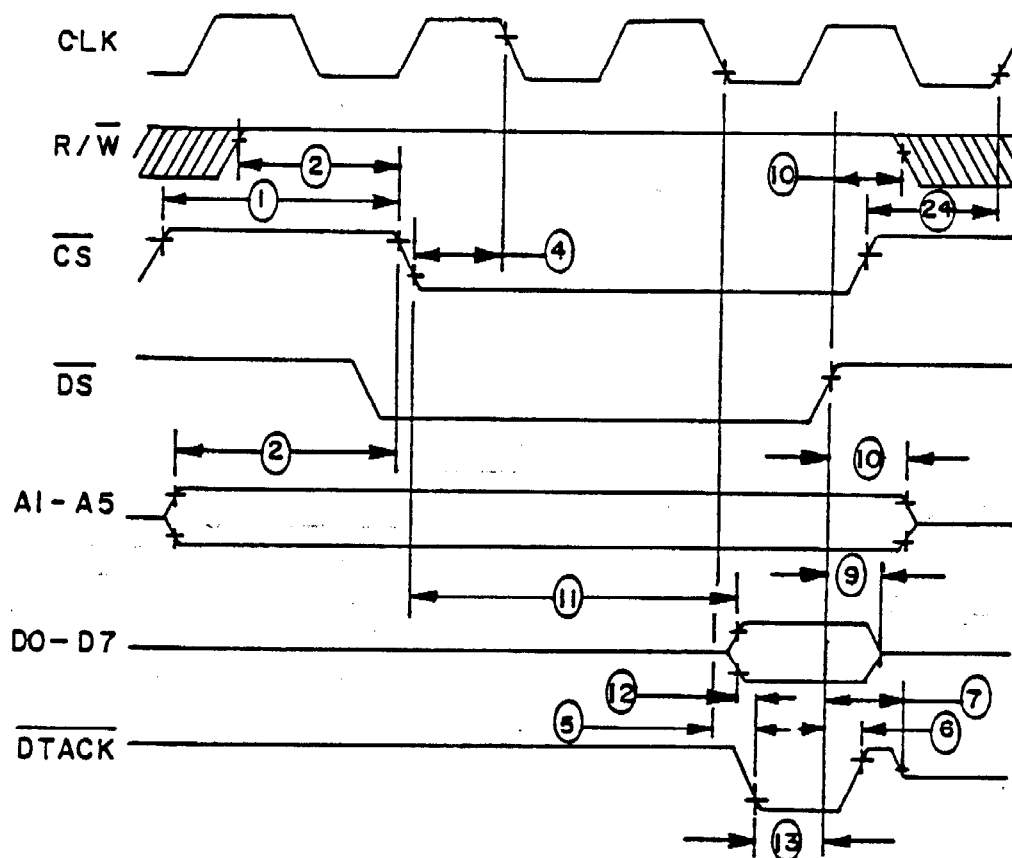
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Read cycle

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V unless otherwise noted.

FIGURE 4. Switching waveforms.

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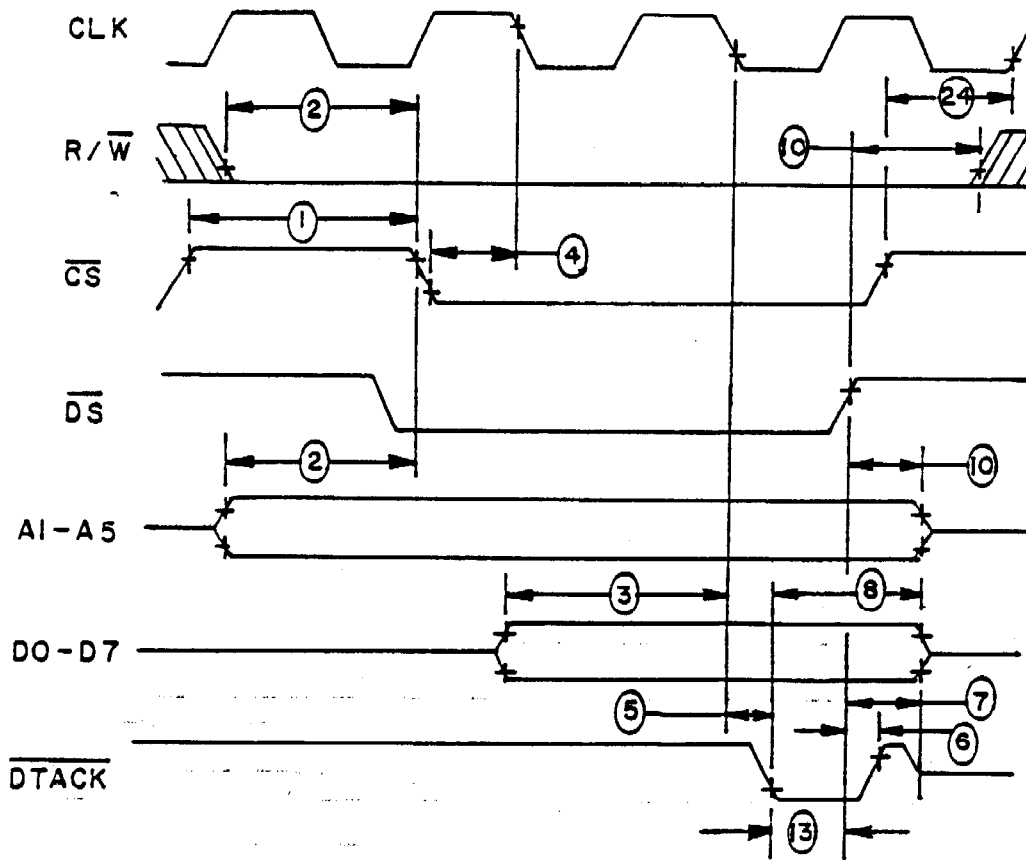
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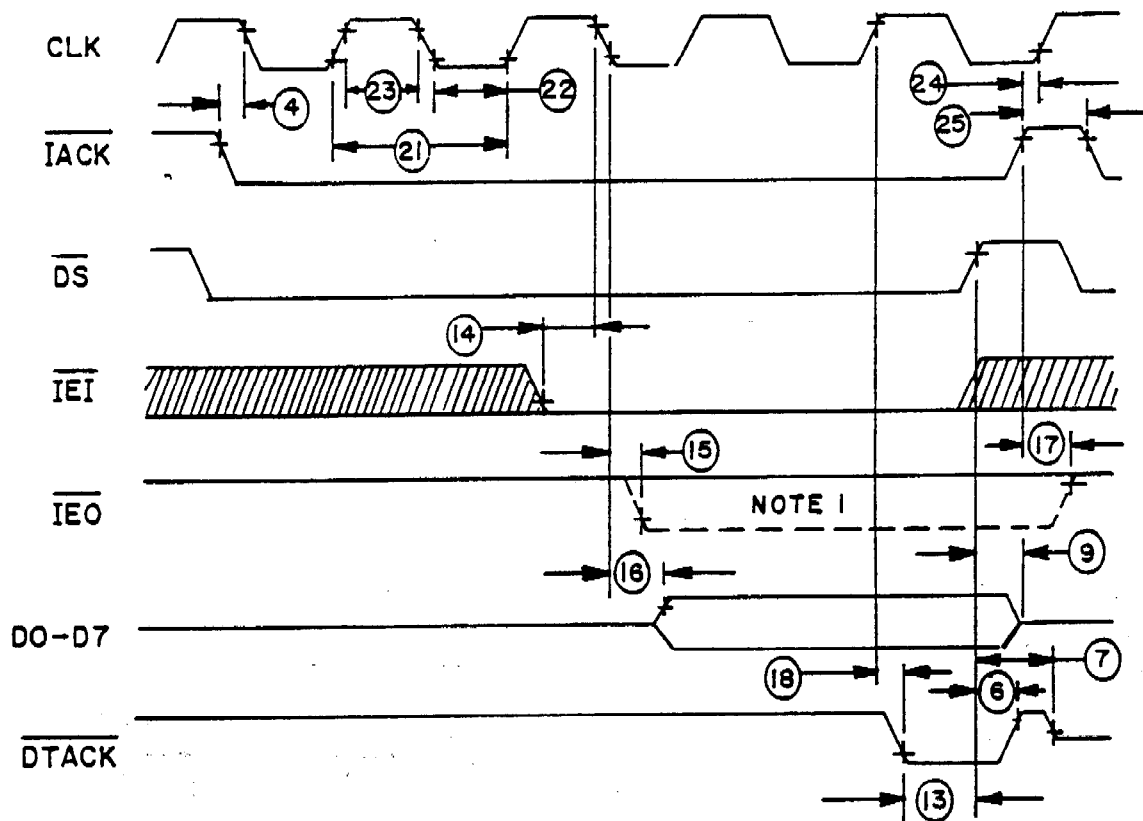


NOTE:
CS and TACK must be a function of DS

Write cycle

FIGURE 4. Switching waveforms - Continued.

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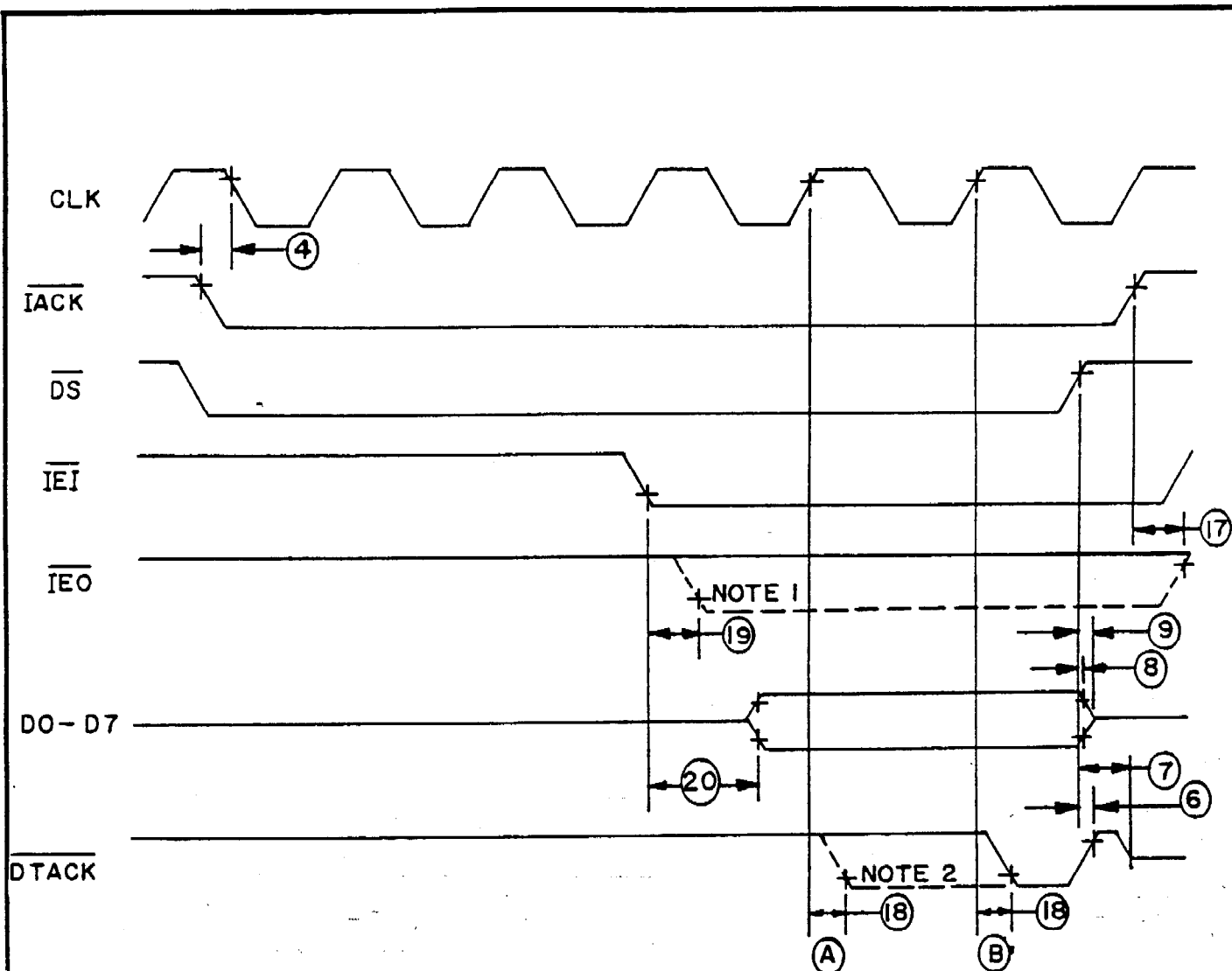


NOTE: \overline{IEO} only goes low if no acknowledgeable interrupt is pending. If \overline{IEO} goes low, \overline{DTACK} and the data bus remain in the high-impedance state.

Interrupt acknowledge cycle (\overline{IEI} low)

FIGURE 4. Switching waveforms - Continued.

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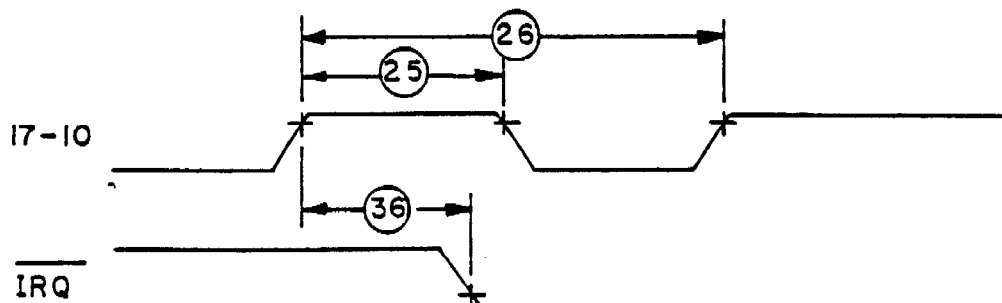


- NOTES: 1. \overline{IEO} only goes low if no acknowledgeable interrupt is pending. If \overline{IEO} goes low, \overline{DTACK} and the data bus remain in the high-impedance state.
2. \overline{DTACK} will go low at (A) if specification number 14 is met. \overline{DTACK} will go low at (B).

Interrupt acknowledge cycle (\overline{IEI} high)

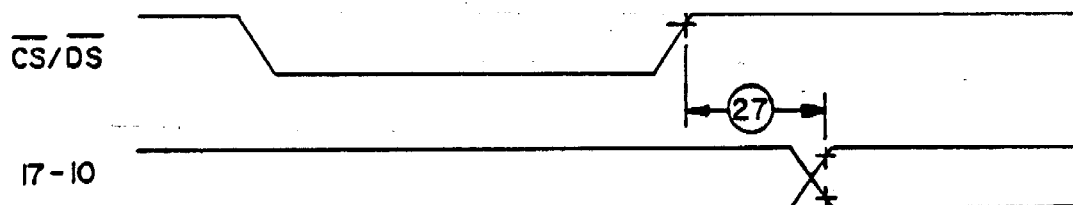
FIGURE 4. Switching waveforms - Continued.

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NOTE:
Active edge is assumed to be the rising edge.

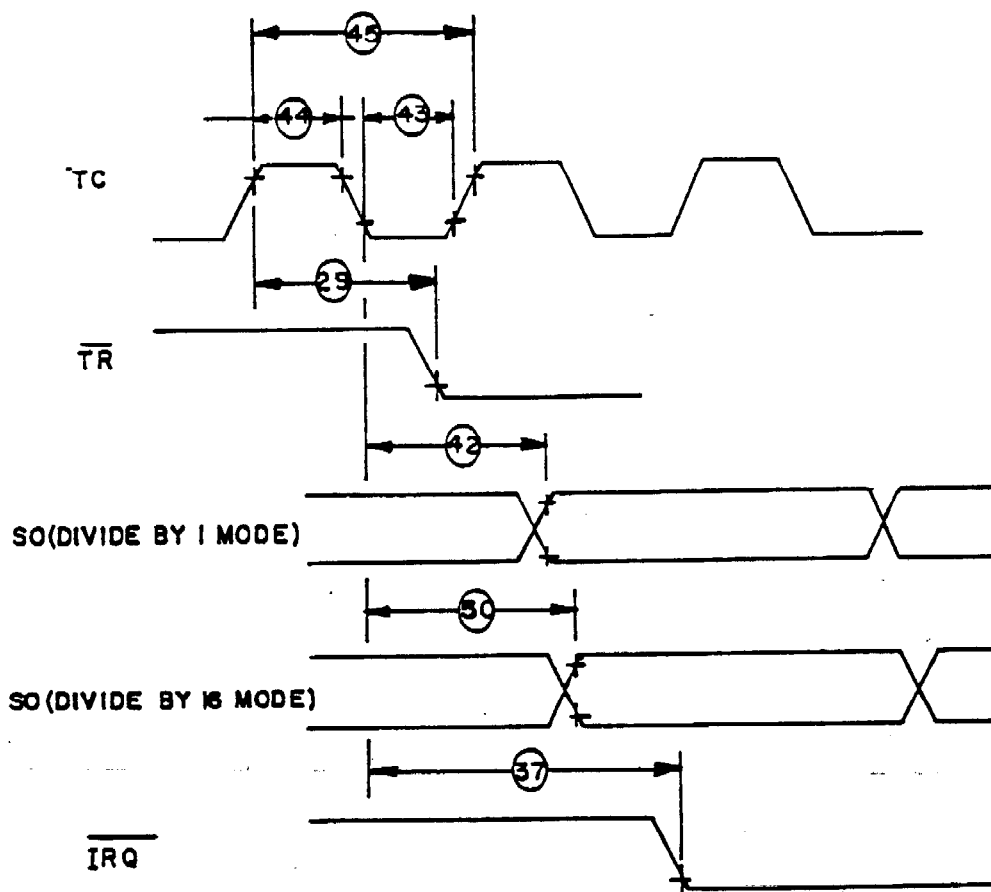
Interrupt timing



Port timing

FIGURE 4. Switching waveforms - Continued.

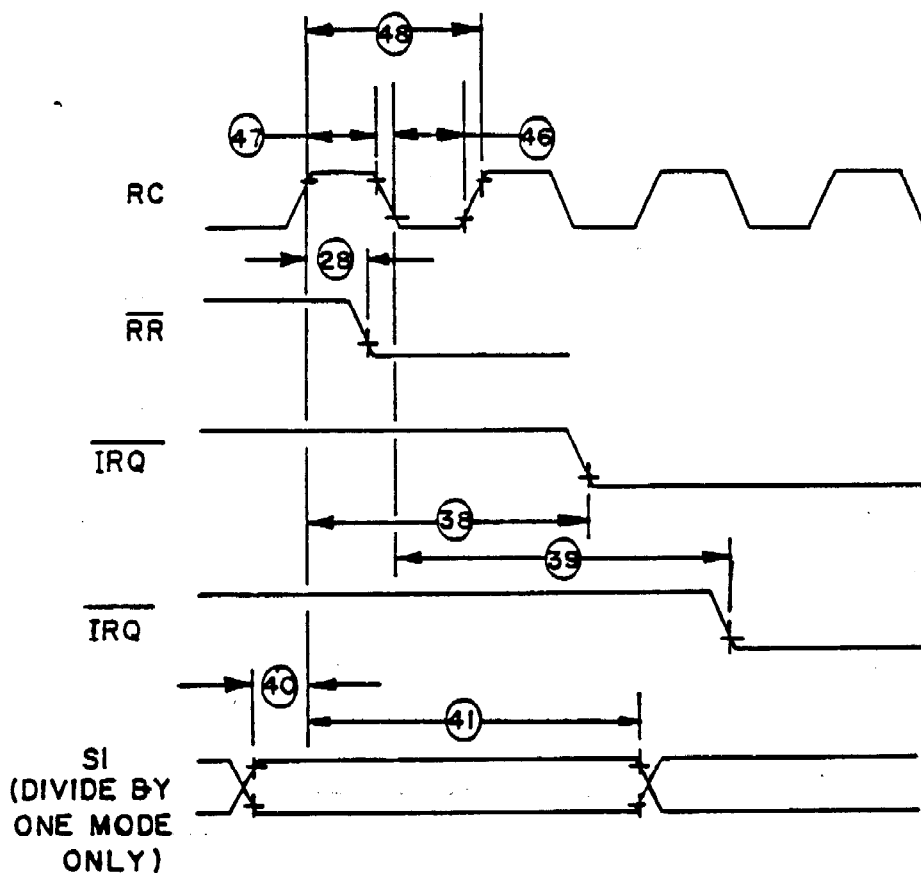
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Transmitter timing

FIGURE 4. Switching waveforms - Continued.

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Receiver timing

FIGURE 4. Switching waveforms - Continued.

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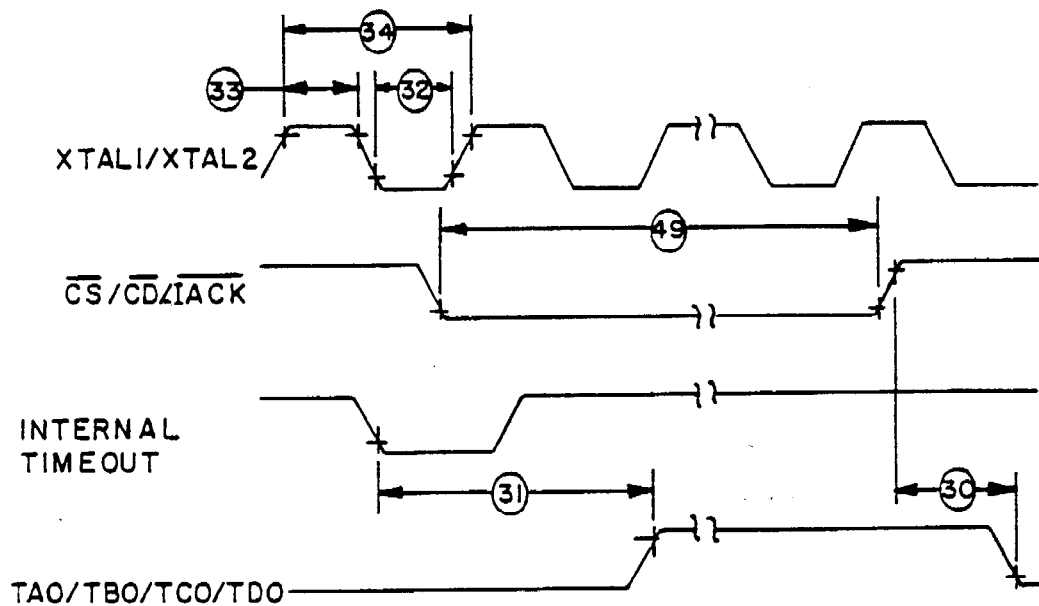
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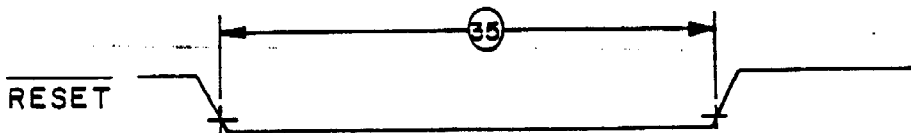
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Timer timing



Reset timing

FIGURE 4. Switching waveforms - Continued.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	2, 8(125°C only), 10

*PDA applies to subgroup 1.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Pin descriptions.

V_{CC} and GND. These inputs supply power to the CMFP. The V_{CC} is power at +5 V and GND is the ground connection.

Clock (CLK). The clock input is a single-phase TTL-compatible signal used for internal timing. This input should not be gated off at any time and must conform to minimum and maximum pulse width times. The clock is not necessarily the system clock in frequency nor phase.

Asynchronous bus control. Asynchronous data transfers are controlled by chip select, data strobe, read/write, and data transfer acknowledge. The low order register select lines, A1-A5, select an internal CMFP register for a read or write operation. The reset line initializes the CMFP registers and the internal control signals.

Chip Select (\overline{CS}). This input activates the CMFP for internal register access.

Data Strobe (\overline{DS}). This input is part of the internal chip select and interrupt acknowledge functions. The CMFP must be located on the lower portion of the 16-bit data bus so that the vector number passed to the processor during an interrupt acknowledge cycle will be located in the low byte of the data word. As a result, \overline{DS} must be connected to the processor's lower data strobe if vectored interrupts are to be used. Note that this forces all registers to be located at odd addresses and latches data on the rising edge for writes. This signal is used as \overline{RD} with an iAPX86 processor type.

Read/Write (R/W). This input defines a data transfer as a read (high) or a write (low) cycle. This signal is used as \overline{WR} with an iAPX86 processor type.

Data Transfer Acknowledge (\overline{DTACK}). This output signals the completion of the operation phase of a bus cycle to the processor. If the bus cycle is a processor read, the CMFP asserts \overline{DTACK} to indicate that the information on the data bus is valid. If the bus cycle is a processor to the CMFP, \overline{DTACK} acknowledges the acceptance of the data by the CMFP. \overline{DTACK} will be asserted only by an CMFP that has \overline{CS} or \overline{IACK} (and \overline{IEI}) asserted. This signal is not used with a 6800 processor type.

Register Select Bus (A1 through A5). The lower five bits of the register select bus select an internal CMFP register during a read or write operation.

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Interrupt Enable Out (\overline{IEO}). This output, together with the \overline{IEI} signal, provides a daisy-chained interrupt structure for a vectored interrupt scheme. The \overline{IEO} of a particular CMFP signals lower priority devices that neither the CMFP nor any other higher-priority device is requesting interrupt service. When a daisy-chain is implemented, \overline{IEO} is tied to the next lower priority device's \overline{IEI} input. The lowest priority device's \overline{IEO} is not connected. When the daisy-chain option is not implemented, \overline{IEO} is not connected.

General purpose I/O interrupt lines (10 through 17). This is an 8-bit pin-programmable I/O port with interrupt capability. The data direction register (DDR) individually defines each line as either a high-impedance input or a TTL-compatible output. As an input, each line can generate an interrupt on the user selected transition of the input signal.

Timer control. These lines provide internal timing and auxiliary timer control inputs required for certain operating modes. Additionally, the timer outputs are included in this group.

Timer clock (XTAL1 and XTAL2). This input provides the timing signal for the four timers. A crystal can be connected between the timer clock inputs, XTAL1 and XTAL2, or XTAL1 can be driven with a TTL-level clock while XTAL2 is not connected. The following crystal parameters are suggested:

- a. Parallel resonance, fundamental mode AT-cut.
- b. Frequency tolerance measured with 18 picofarads load (0.1 percent accuracy) - drive level 10 microwatts.
- c. Shunt capacitance equals 7 picofarads maximum.
- d. Series resistance:
 $2.0 < f < 2.7 \text{ MHz}; RS \leq 300\Omega$
 $2.8 < f < 4.0 \text{ MHz}; RS \leq 150\Omega$

Timer inputs (TAI and TBI). These inputs are control signals for timers A and B in the pulse width measurement mode and event count mode. These signals generate interrupts at the same priority level as the general purpose I/O interrupt lines 14 and 13, respectively. While 14 and 13 do not have interrupt capability when the timers are operated in the pulse width measurement mode or the event count mode, 14 and 13 may still be used for I/O.

Timer outputs (TAO, TBO, TCO, and TDO). Each timer has an associated output which toggles when its main counter counts through 01 (hexadecimal), regardless of which operational mode is selected. When in the delay mode, the timer output will be a square wave with a period equal to two timer cycles. This output signal may be used to supply the universal synchronous/asynchronous receiver-transmitter (USART) baud rate clocks. Timer outputs TAO and TBO may be cleared at any time by writing a one to the reset location in timer control registers A and B. Also, a device reset forces all timer outputs low.

Data bus (D0 through D7). This bidirectional bus is used to receive data from or transmit data to the CMFP's internal registers during a processor read or write cycle. During an interrupt acknowledge cycle, the data bus is used to pass a vector number to the processor. Since the CMFP is an 8-bit peripheral, the CMFP could be located on either the upper or lower portion of the 16-bit data bus (even or odd address). However, during an interrupt acknowledge cycle, the vector number passed to the processor must be located in the low byte of the data word. As a result, D0-D7 of the CMFP must be connected to the low order eight bits of the processor data bus, placing CMFP registers at odd addresses if vectored interrupts are to be used.

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Reset (**RESET**). This input will initialize the CMFP during power-up or in response to a total system reset.

Interrupt control. The interrupt request and interrupt acknowledge signals are handshake lines for a vectored interrupt scheme. Interrupt enable in and the interrupt enable out implement a daisy-chained interrupt structure.

Interrupt Request (**IRQ**). This output signals the processor that an interrupt is pending from the CMFP. These are 16 interrupt channels that can generate an interrupt request. Clearing the interrupt pending registers (IPRA and IPRB) or clearing the interrupt mask registers (IMRA and IMRB) will cause **IRQ** to be negated. **IRQ** will also be negated as the result of an interrupt acknowledge cycle, unless additional interrupts are pending in the CMFP.

Interrupt Acknowledge (**IACK**). If both **IRQ** and **IEI** are active, the CMFP will begin an interrupt acknowledge cycle when **IACK** and **DS** are asserted. The CMFP will supply a unique vector number to the processor which corresponds to the interrupt handler for the particular channel requiring interrupt service. In a daisy-chained interrupt structure, all devices in the chain must have a common **IACK**.

Interrupt Enable In (**IEI**). This input, together with the **IEO** signal, provides a daisy-chained interrupt structure for a vectored interrupt scheme. **IEI** indicates that no higher priority device is requesting interrupt service. So, the highest priority device in the chain should have its **IEI** pin tied low. During an interrupt acknowledge cycle, an CMFP with a pending interrupt is not allowed to pass a vector number to the processor until its **IEI** pin is asserted. When the daisy-chain option is not implemented, all CMFPs should have their **IEI** pin tied low.

Serial I/O control. The full duplex serial channel is implemented by a serial input and output line. The independent receive and transmit sections may be clocked by separate timing signals on the receiver clock input and the transmitter clock input.

Serial Input (**SI**). This input line is the USART receiver data input. This input is not used in the USART loopback mode.

Serial Output (**SO**). This output line is the USART transmitter data output. This output is driven high during a device reset.

Receiver Clock (**RC**). This input controls the serial bit rate of the receiver. This signal may be supplied by the timer output lines or by any external TTL-level clock which meets the minimum and maximum cycle times. This clock is not used in the USART loopback mode.

Transmitter Clock (**TC**). This input controls the serial bit rate of the transmitter. This signal may be supplied by the timer output lines or by an external TTL-level clock which meets the minimum and maximum cycle times.

DMA control. The USART supports DMA transfers through its receiver ready and transmitter ready status lines.

Receiver Ready (**RR**). This output reflects the receiver buffer full status for DMA operations.

Transmitter Ready (**TR**). This output reflects the transmitter buffer empty status for DMA operations.

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6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>	Replacement military specification part number
5962-8850601XX	50088	TS68901MCB/C4	---
5962-8850601YX	50088	TS68901MEB/C4	---
5962-8850602XX	50088	TS68901MCB/C5	---
5962-8850602YX	50088	TS68901MEB/C5	---

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

50088

Vendor name
and address

Thomson-Components-Mostek Corporation
P.O. Box 169
1310 Electronics Drive
Carrollton, TX 75006

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